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Hangzhou CloudSemi Technology Co., Ltd

GaN Switching Behavior Analysis

GaN Device R&D Team

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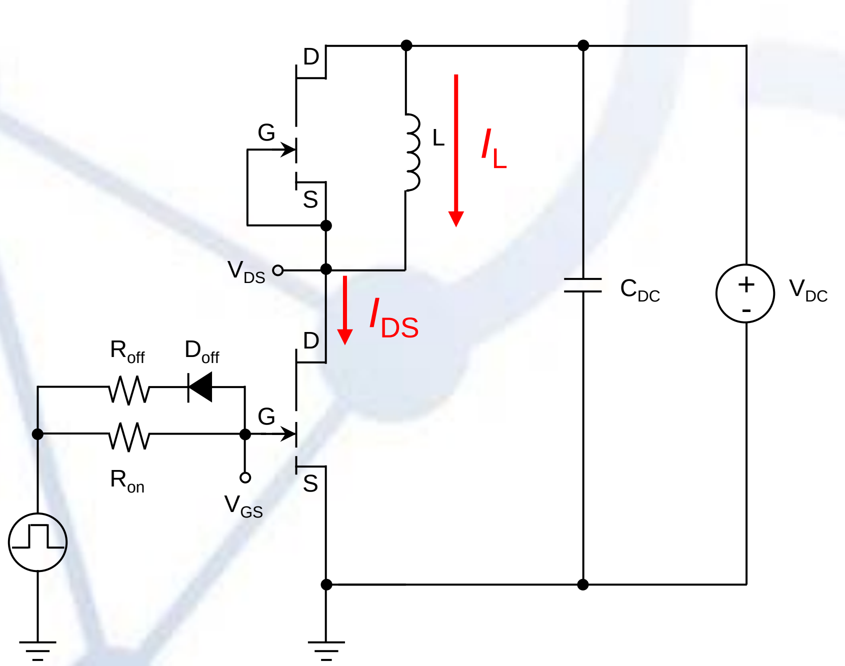
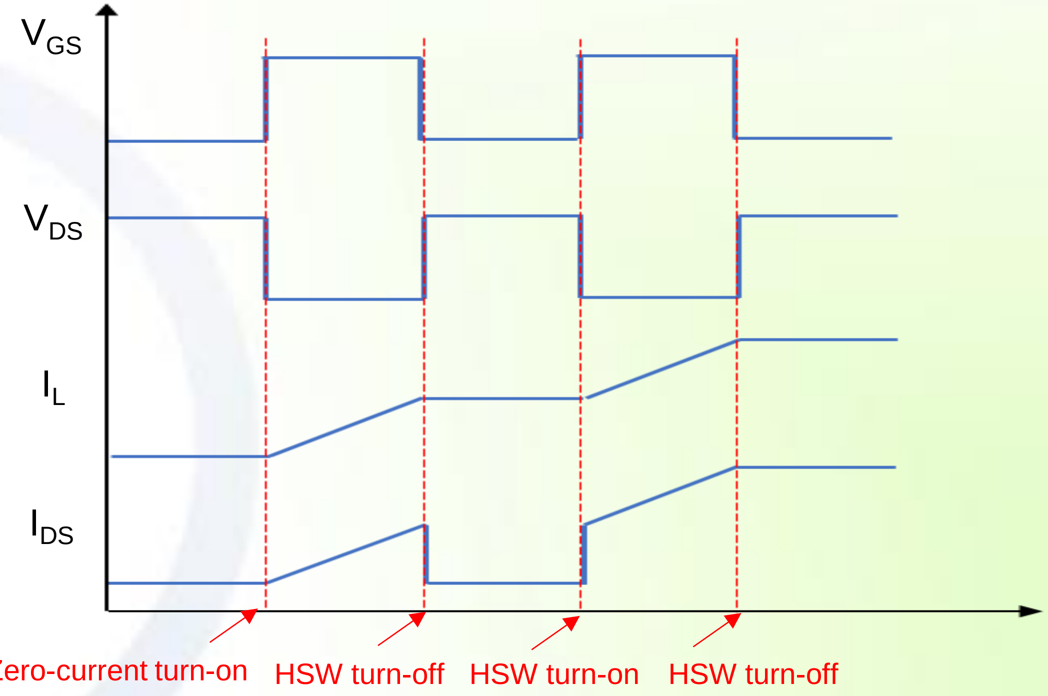
Powering the Dreams!

Double pulse tester for GaN FET

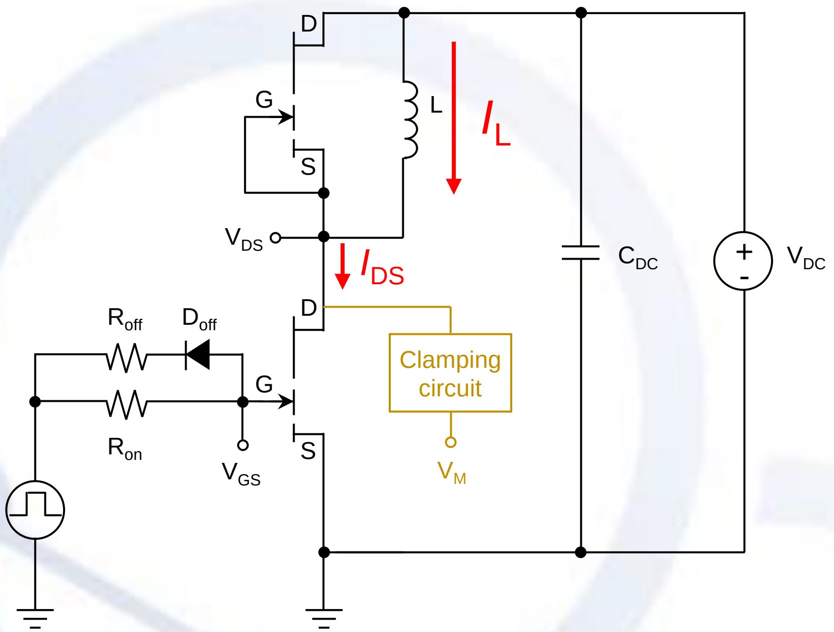
Why do we need double pulse tester to measure GaN FETs?

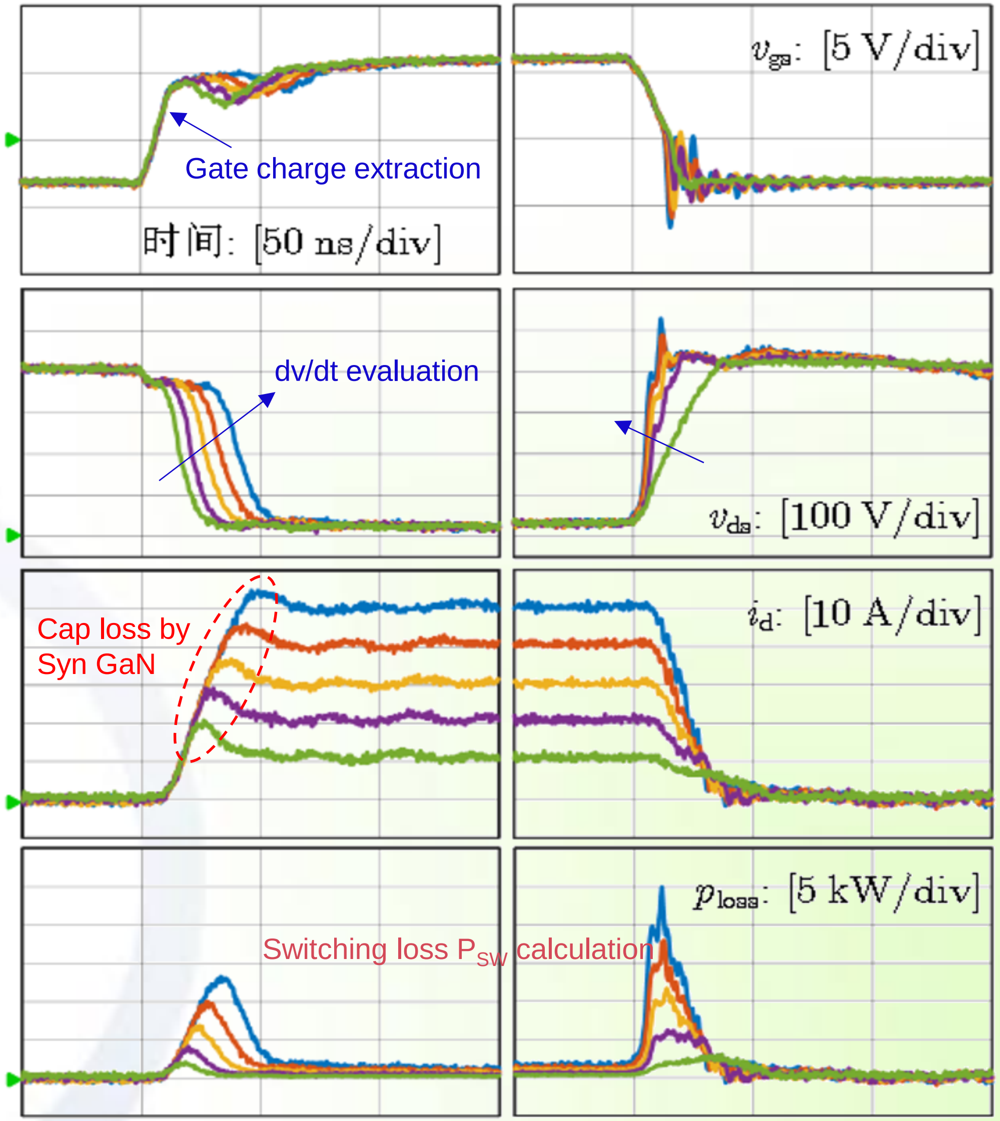
1. Extracting GaN switching parameters (t_{on}, t_{off}, t_r, t_f)
2. Extracting GaN switching loss (E_{on}, E_{off})
3. Emulating the system behavior, e.g. turn-off drain spike, switching time, gate ringing and etc.
4. Evaluating the dynamic performance of GaN, e.g. dynamic R_{dson}, HSW D-HTOL, switching SOA, and etc.
5. No need of high-power equipment, low-cost scheme





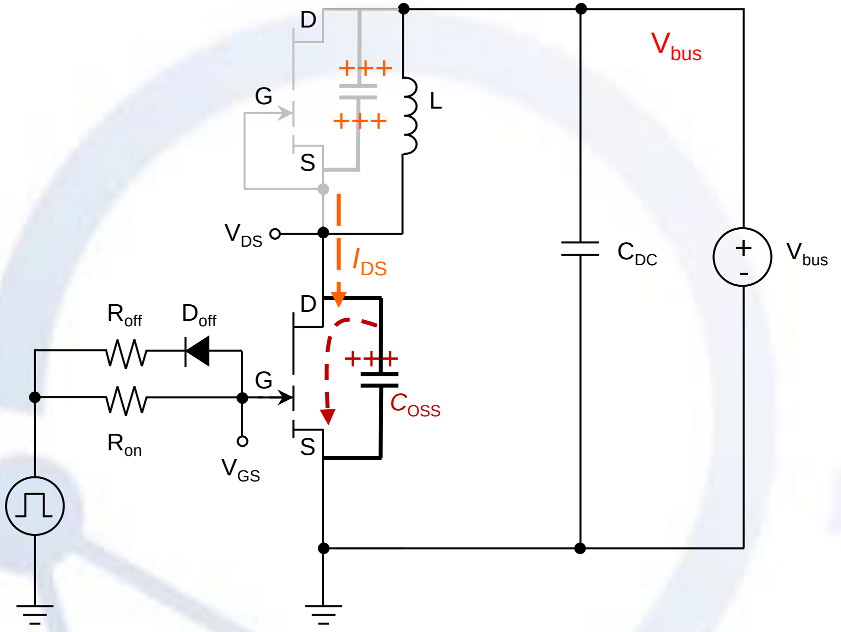
Double pulse tester for GaN FET: example

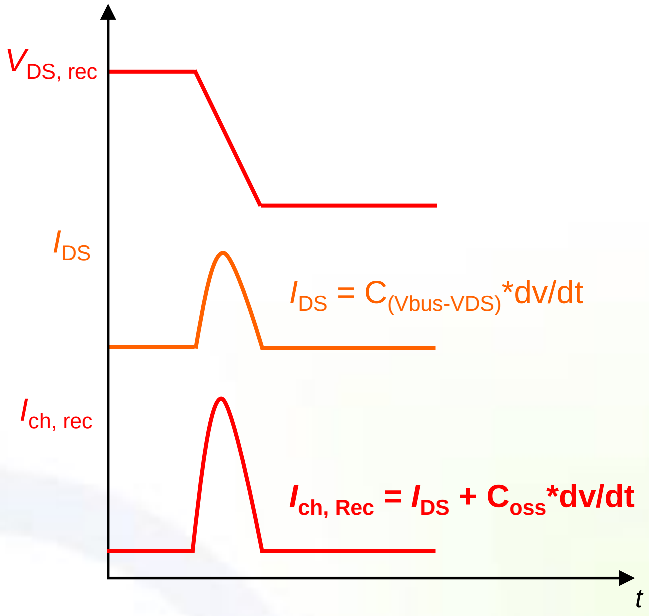


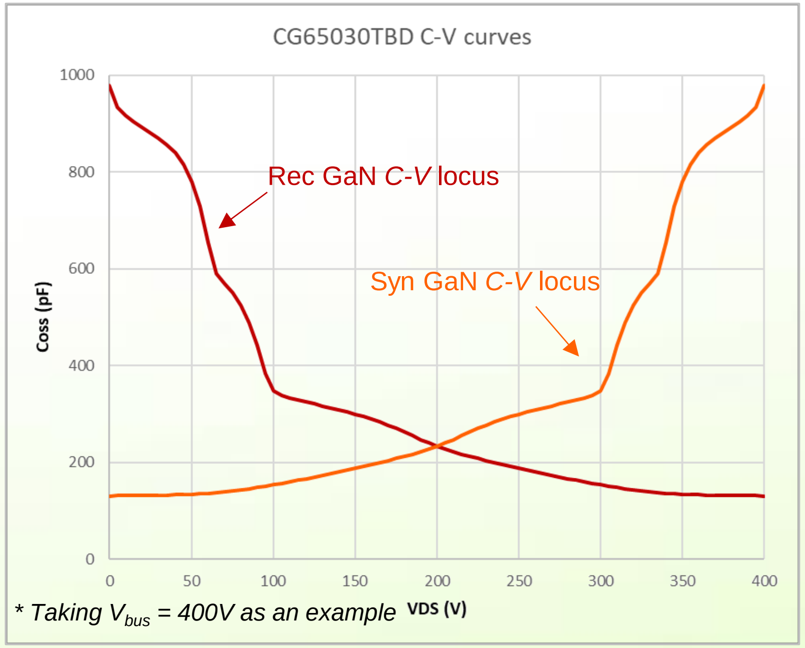


- 650V/30mΩ CloudSemi E-mode GaN device under test
- Stable switching behavior from HSW DPT test
- Nearly all the dynamic parameters can be extracted from measurement
- Additionally implemented clamping circuit can assist to extract the dynamic R_{dson}

1st pulse turn-on: zero-current capacitive load



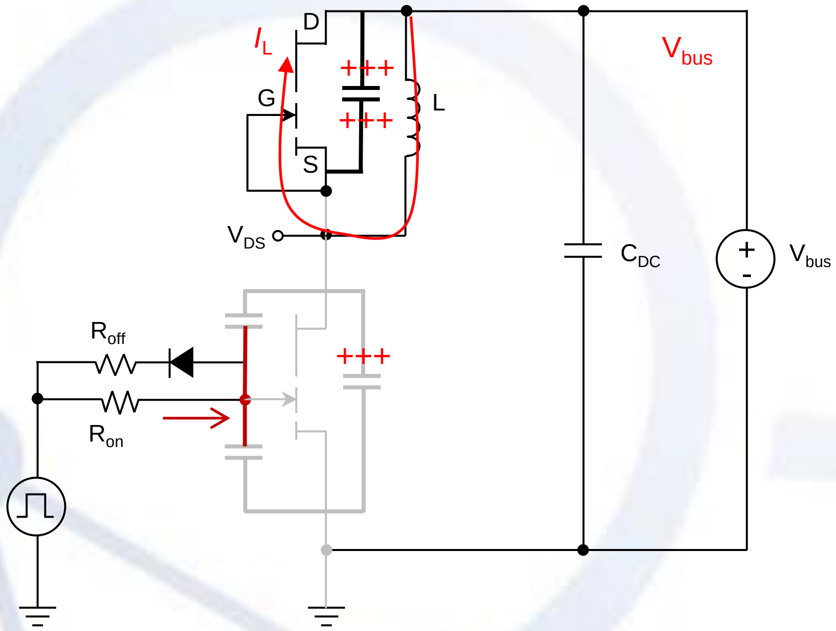


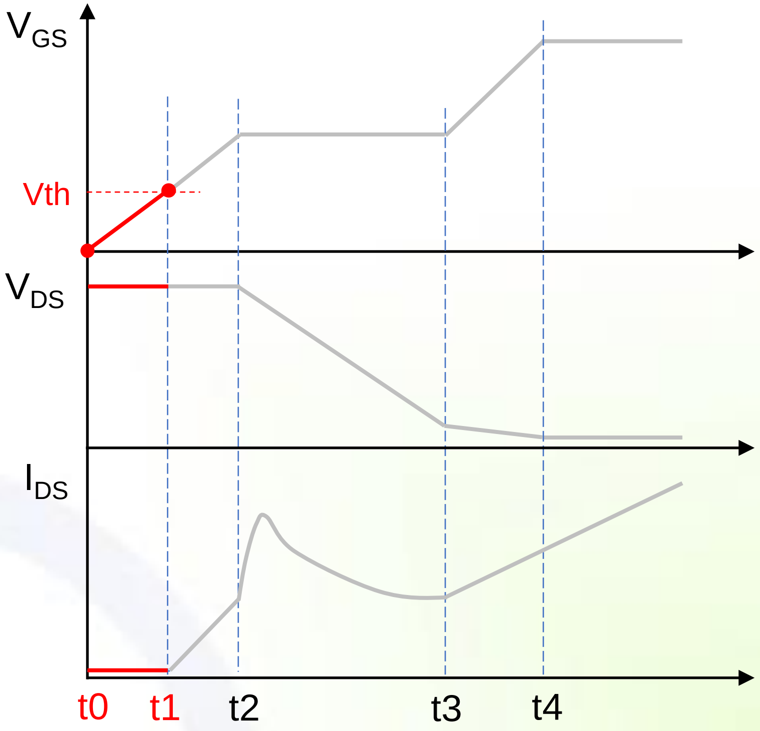


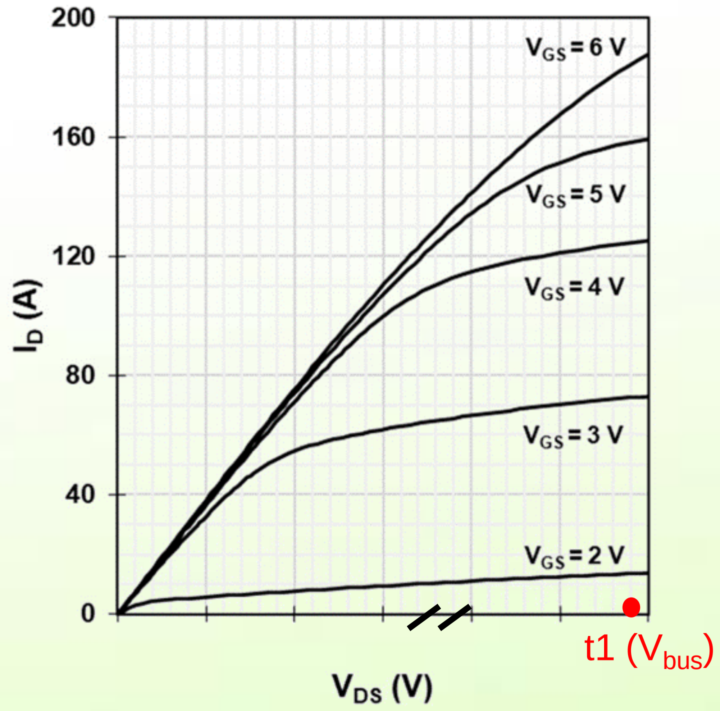
Stage of start-up, zero-current turn-on (capacitive-load switching):

- V_{DS} of rectifier transistor (low-side GaN in this slide): $V_{bus} \rightarrow 0$; V_{DS} of synchronous transistor (high-side GaN in this slide): $0 \rightarrow V_{bus}$
- The setup can be treated as a capacitive-load switching:
  - Oscilloscope-captured I_{DS} comes from charging C_{OSS} of Syn GaN: $I_{DS} = C_{(Vbus\text{-}VDS)}$*dv/dt
  - Displacement current of discharging C_{OSS} of Rec GaN cannot be directly captured by oscilloscope: $I_{Coss} = C_{oss}$*dv/dt
  - Current through Rec GaN channel consists of two part above: **$I_{ch,\ Rec} = I_{DS} + C_{oss}$*dv/dt**
- $Cap\ Loss(Rec\ FET) = \int_0^{V_{bus}} C_{OSS} * V_{DS}\, dV$ $\quad Cap\ Loss(Syn\ FET) = \int_0^{V_{bus}} C_{OSS} * (V_{bus} - V_{DS}) dV = V_{bus} * Q_{oss} - \int_0^{V_{bus}} C_{OSS} * V_{DS}\, dV$ $\quad \boxed{\boldsymbol{Total\ cap\ Loss = V_{bus} * Q_{oss}}}$

HSW turn-on transient: Vgoff to Vth



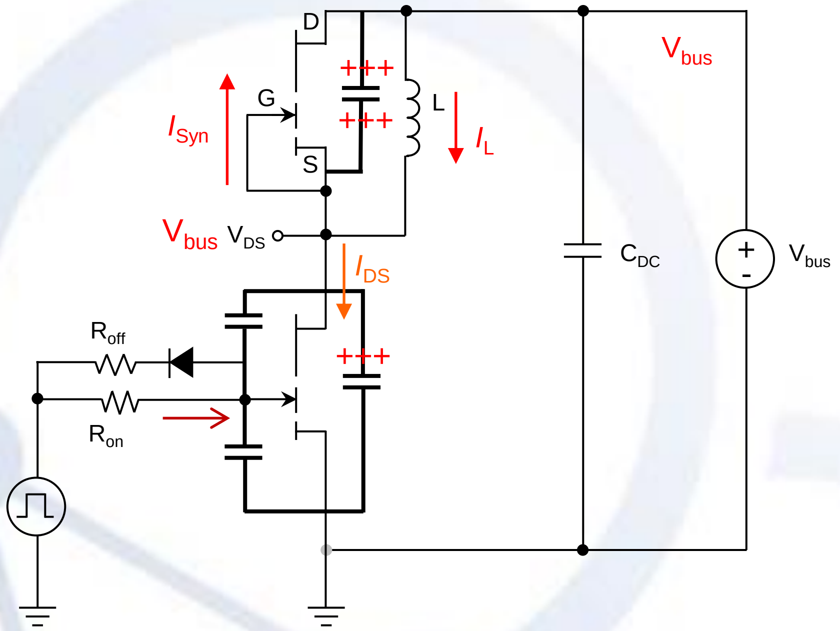


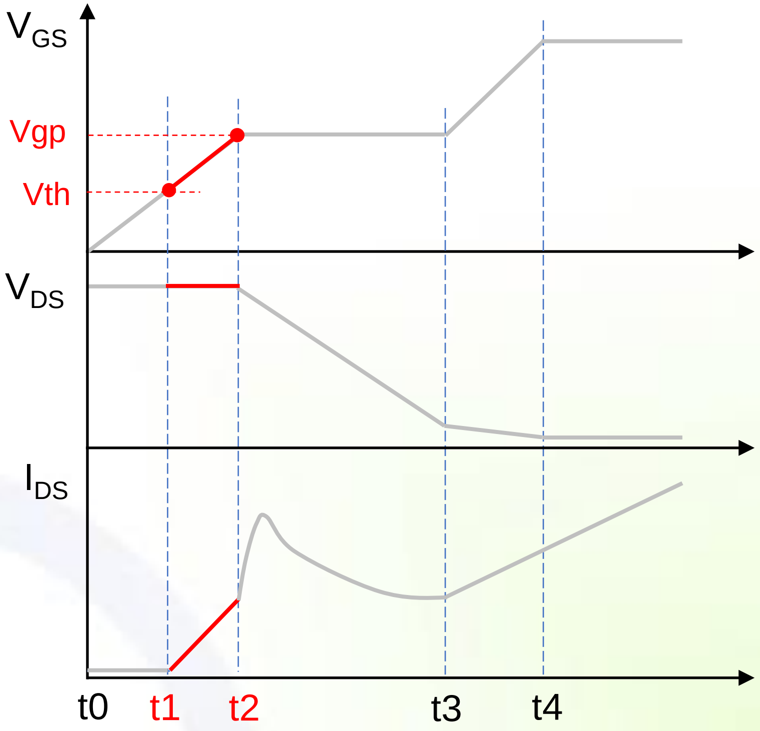


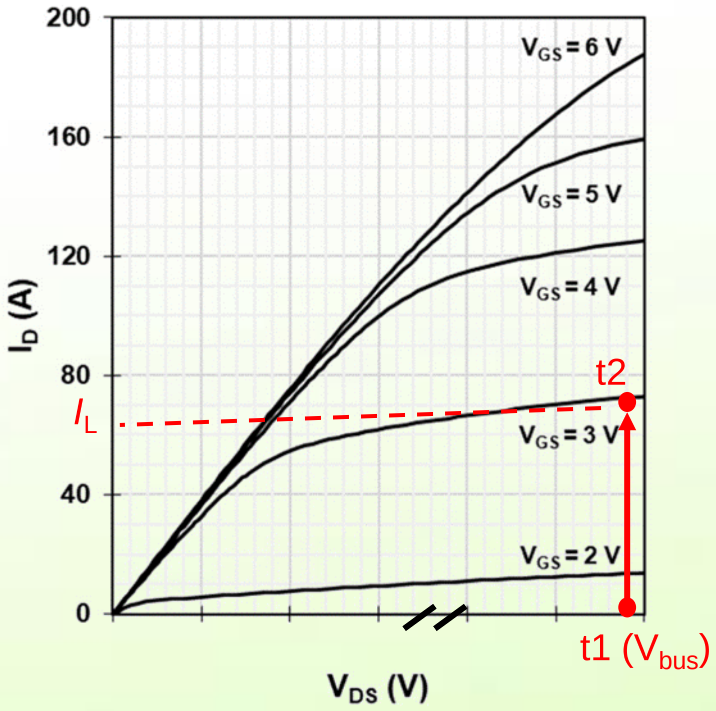
t0~t1, gate drive charges Ciss of Rec GaN:

- V_{GS} of Rec GaN rises from 0 to Vth, and V_{DS} = V_{bus}. No current flows through Rectifier GaN.
- Load current flows through inductor and Syn GaN.
- Until V_{GS} of Rec GaN reaches to its Vth, load current starts to commutate and flows through it.

HSW turn-on transient: current commutation



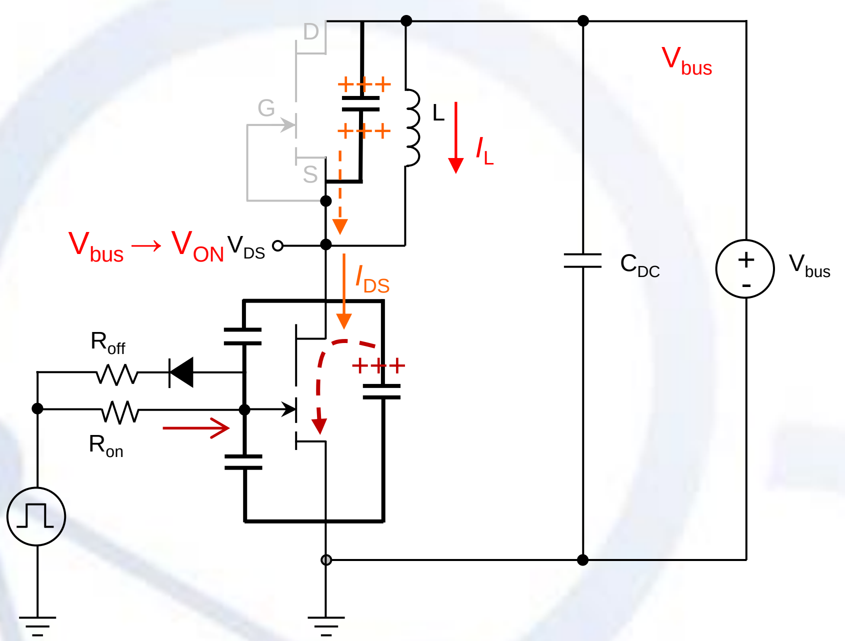


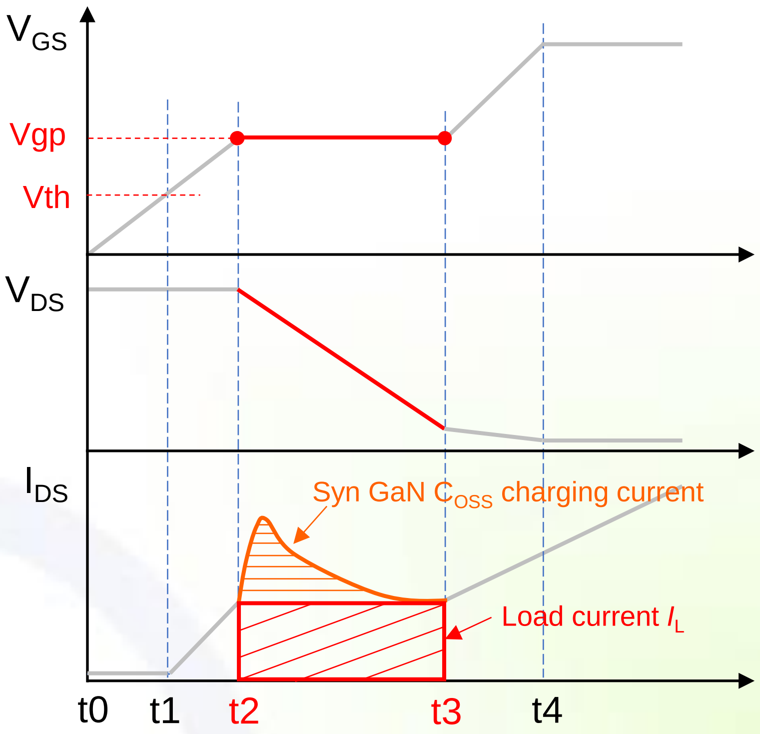


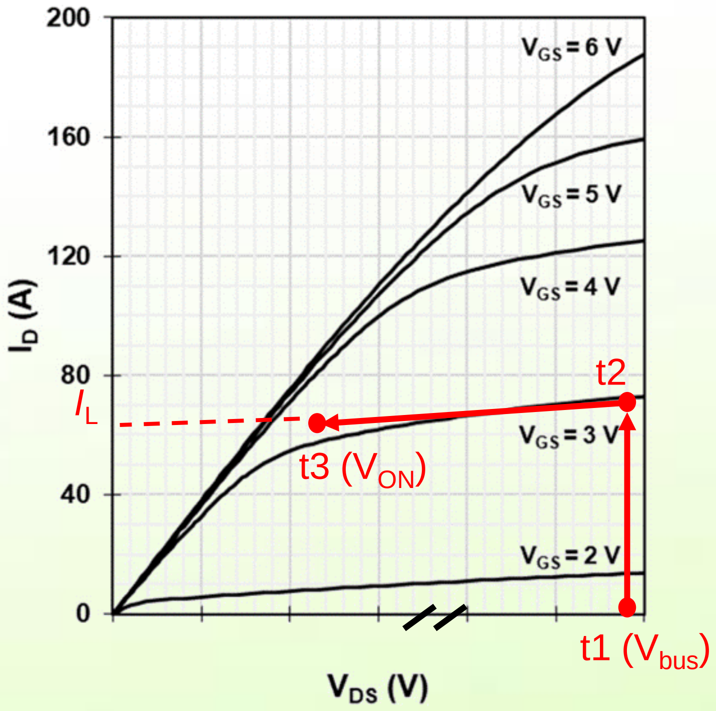
t1~t2, current commutation [load current commutates from Syn GaN to Rec GaN]:

- As V_{GS} of Rec GaN reaches its Vth, current starts to flow through Rec GaN. Load current gradually commutates from Syn GaN to Rec GaN, as V_{GS} increases;
- During current commutation, the gate driver charges Ciss until Rec GaN has current capability of I_L. [**$I_{DS,\ VGS=Vgp} = I_L$**]
- When V_{GS} = Vgp (Miller plateau, = Vth + I_L/g_m), all the inductive-load current flows through the Rec GaN.
- In this duration, Rec GaN I_{DS} overlaps with V_{DS}, and **I-V overlap loss** dominates and can be calculated by integrating I & V.

HSW turn-on transient: voltage commutation



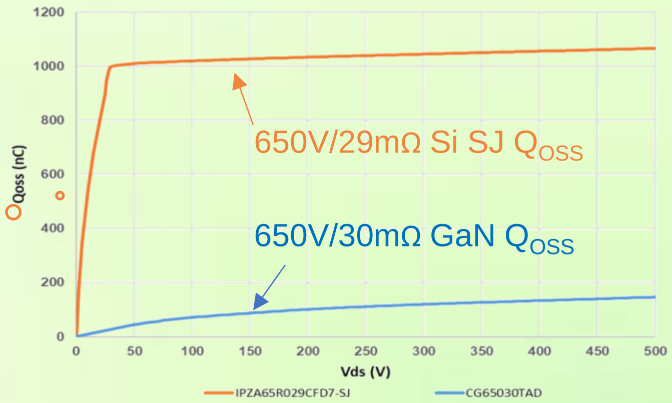




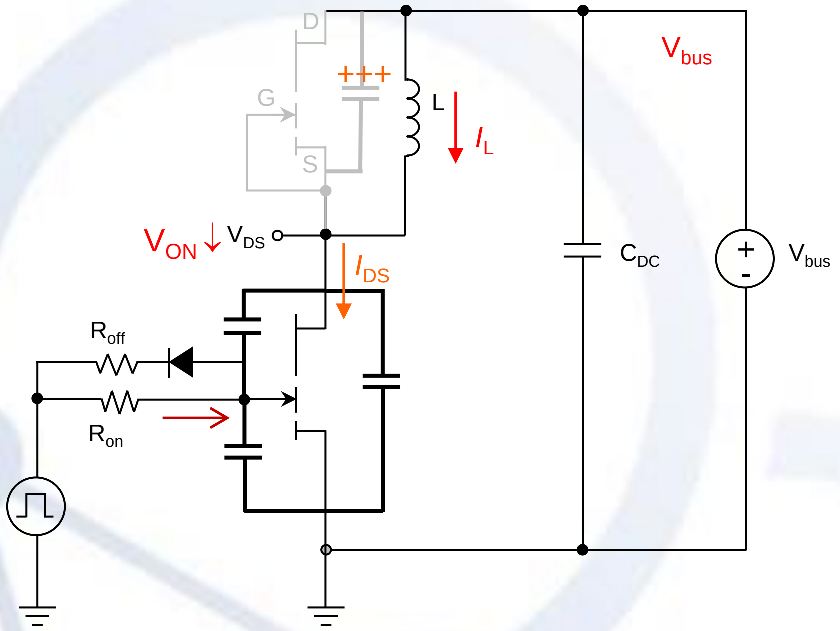
t2~t3, voltage commutation [Rec GaN V_{DS} drops to $V_{ON} = I_L{*}R_{dson}(V_{GS}=Vgp)$]:

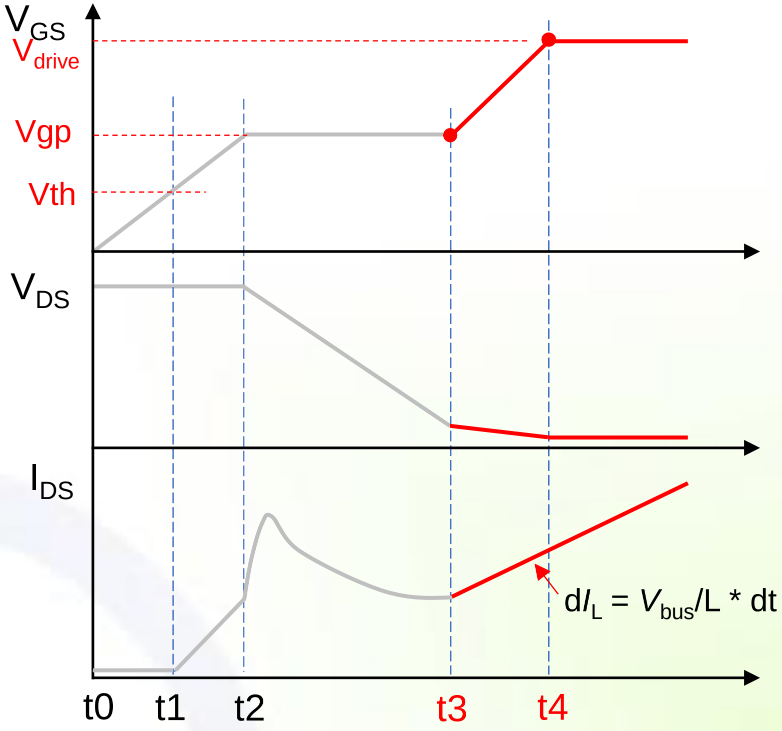
- As V_{GS} of Rec GaN reaches Vgp, all the inductive-load current flows through Rec GaN;
- Then, Rec GaN C_{OSS} starts to discharge from V_{bus} to V_{ON} & Syn GaN C_{OSS} starts to charge to V_{bus}
- Rec GaN C_{OSS} discharging cannot be captured, but Syn GaN C_{OSS} charging can be recognized from I_{DS} waveform
- During this duration, the loss on Rec GaN consists of **2 main parts**:
  - I-V overlap loss
  - Cap loss from Syn/Rec GaN charging/discharging: $V_{bus}{*}Q_{OSS}$ (if Syn/Rec GaN feature the same part number)

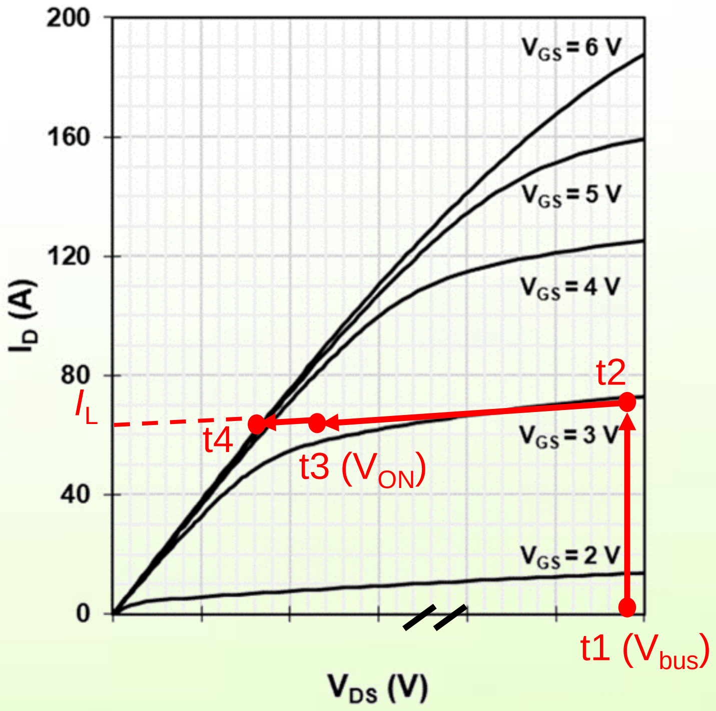
GaN features much lower Q_{OSS} and switching loss

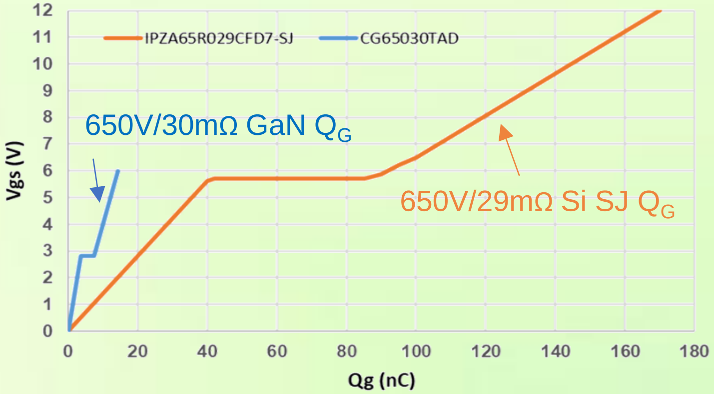


HSW turn-on transient: gate over-drive





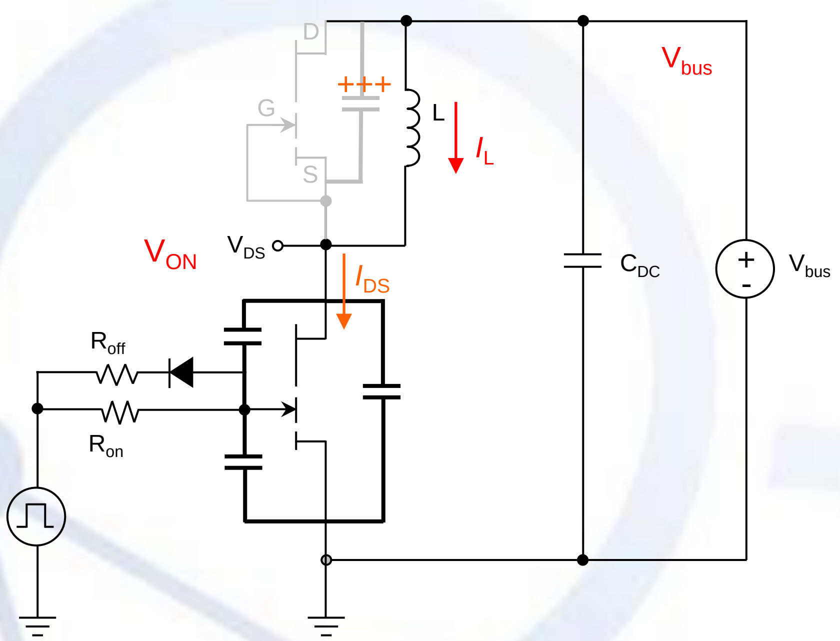


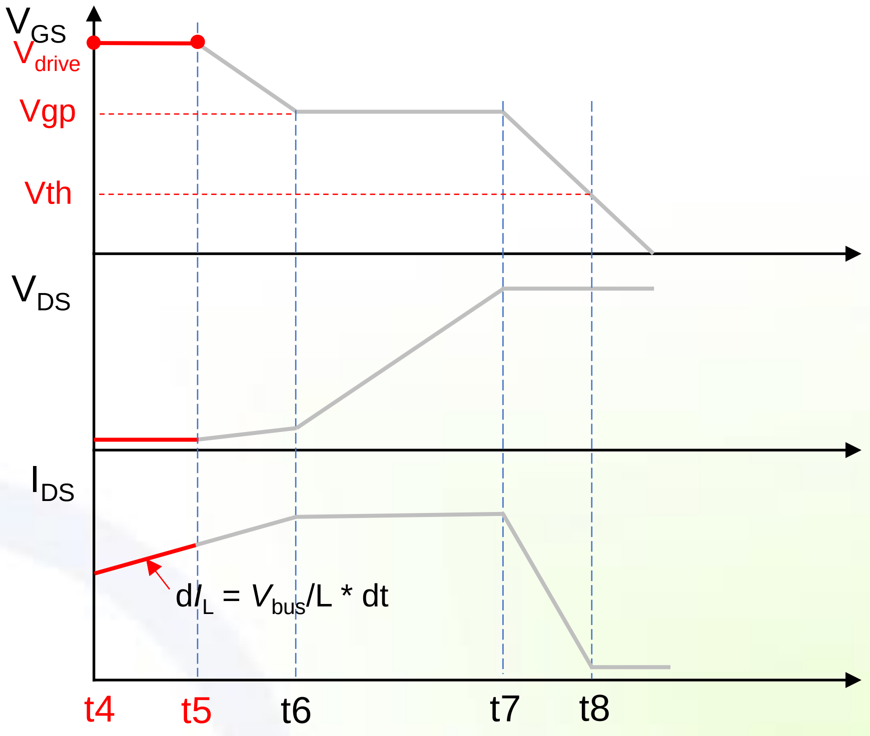


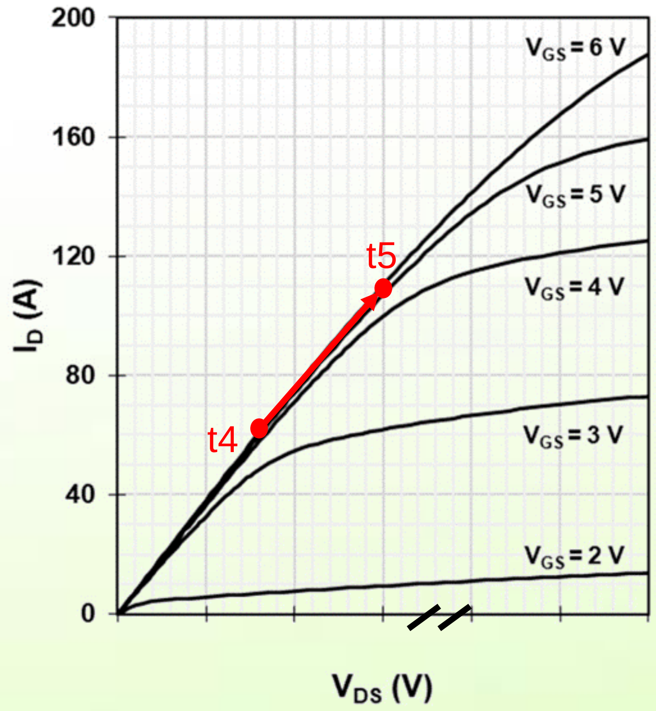
t3~t4, gate over-drive to make GaN fully turn-on:

- Gate driver continues to charge Ciss from Vgp to V_{drive} (e.g. 6V), making GaN FET fully turn-on
- Comparing to Si SJ, GaN FET features much lower gate charge Q_G (as shown in right plot)
- $V_{ON} = I_L * R_{dson}$ ($V_{GS} = V_{drive}$). The recommended gate drive voltage for CloudSemi E-mode GaN FET is 5.5~6.5V.
- After t4, inductive load will continue to excite, following $dI_L = V_{bus}/L * dt$
- Conduction loss on Rec GaN FET dominates in this duration

Turn-on period: excitation







t4~t5, inductive load excitation:

- $dI_L = V_{bus}/L * dt$, $I_{DS} = I_L$
- Ciss stops charging
- Current flowing through GaN channel gradually increases
- Rec GaN FET works in linear region.
- Conduction loss on Rec GaN FET dominates in this duration

HSW turn-off transient: $V_{GS} \rightarrow$ Vgp

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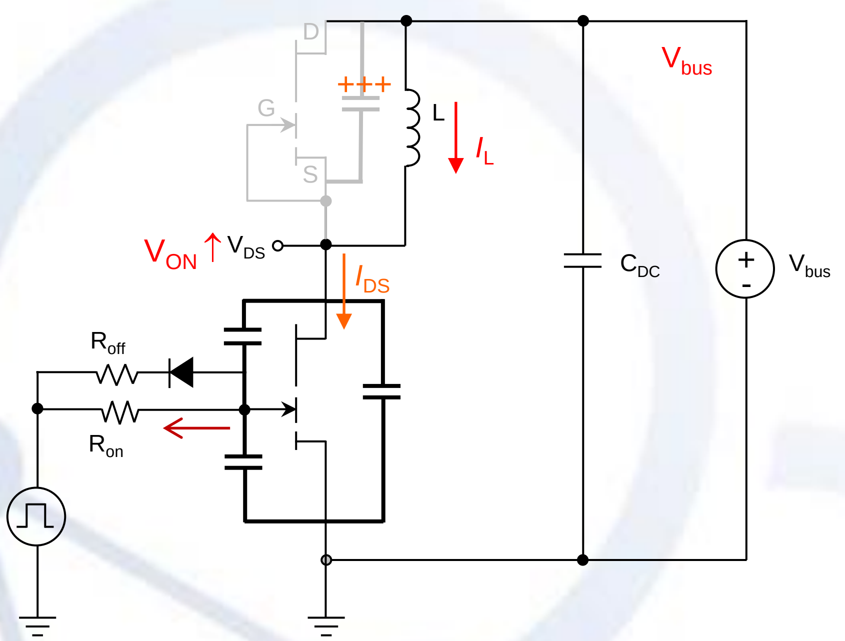

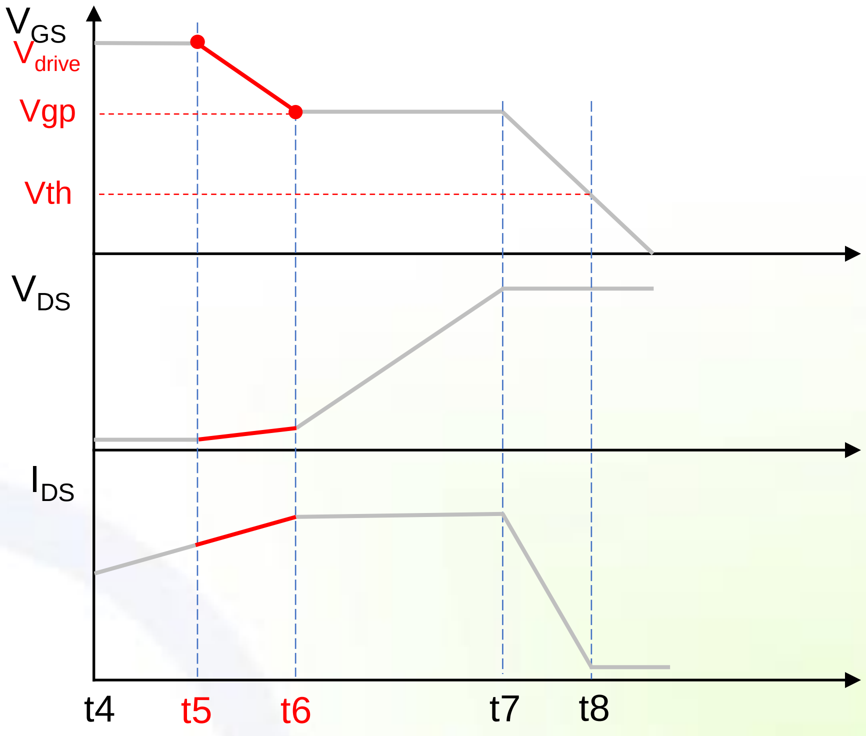

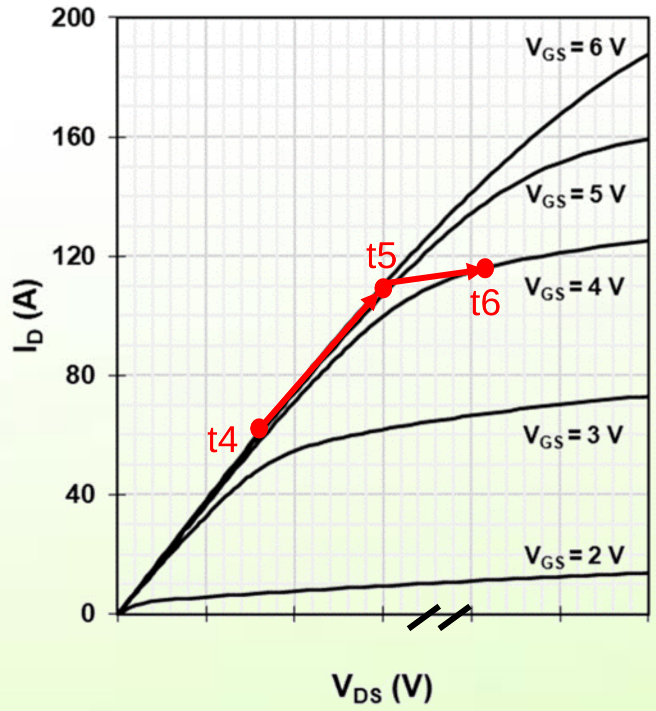

t5~t6, Ciss starts discharging:

- Ciss of Rec GaN starts to discharge, until GaN enters saturation mode (V_{GS} = Vgp, I_{dsat} = I_L).
- Here, Vgp = Vth + I_L/g_m
- Rec GaN FET works from linear region to saturation region (as output curves in this slide)
- Conduction loss on Rec GaN FET dominates in this duration

HSW turn-off transient: voltage commutation

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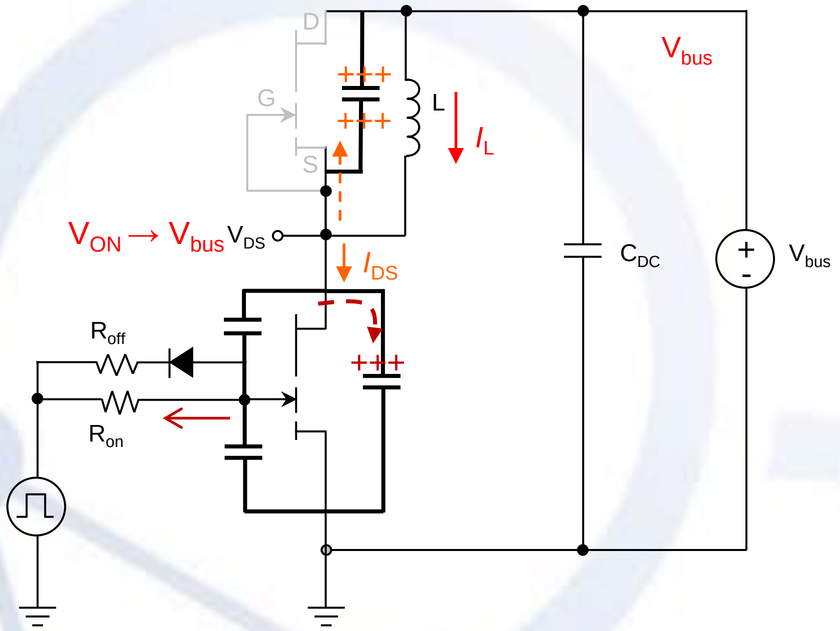
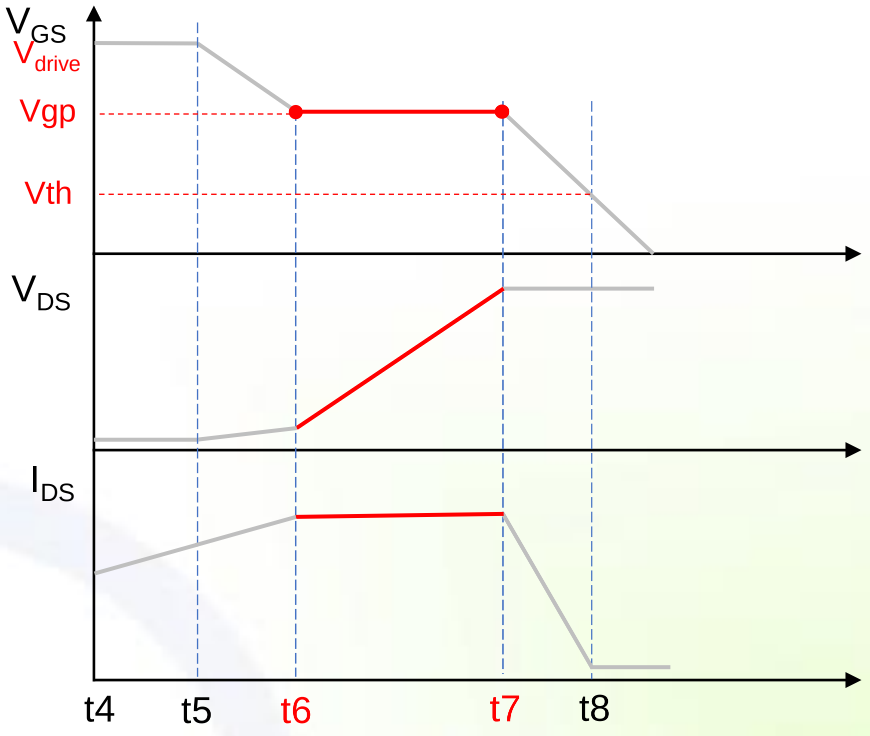
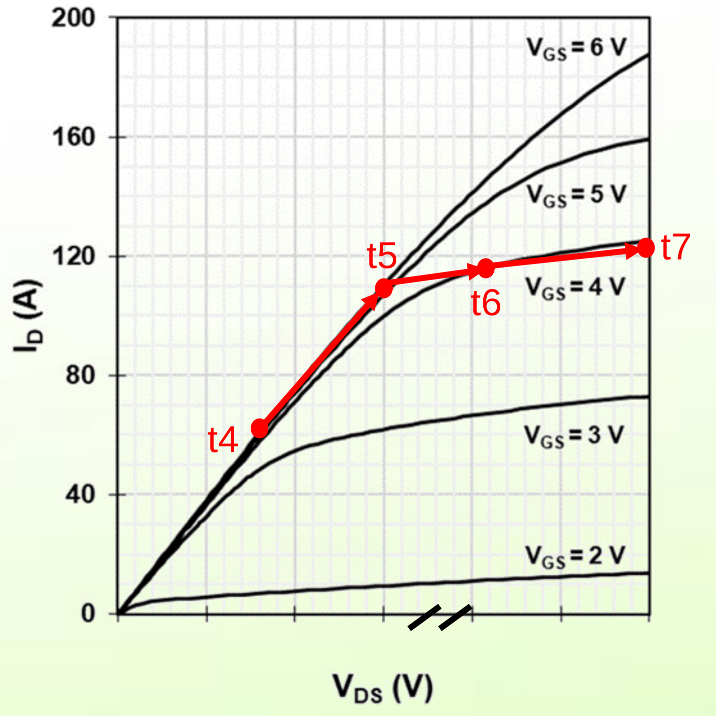


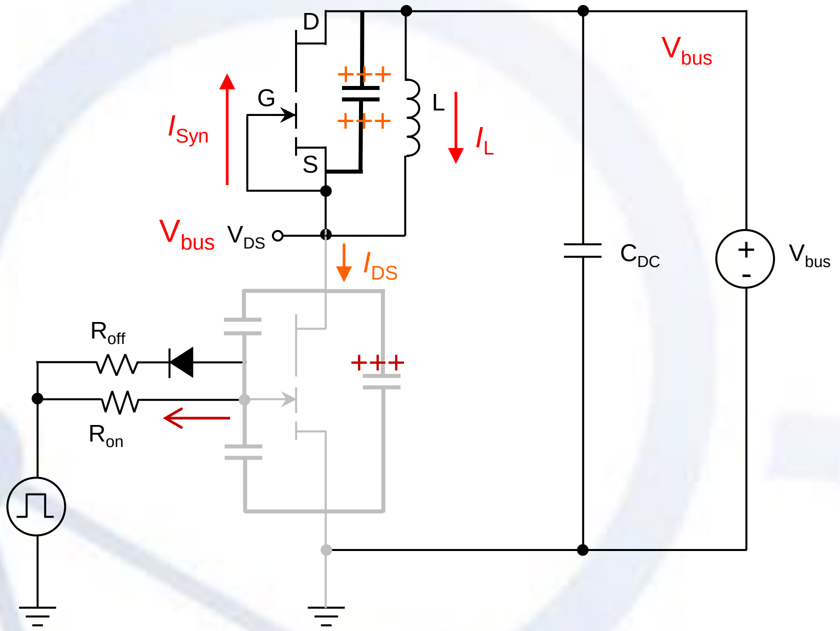


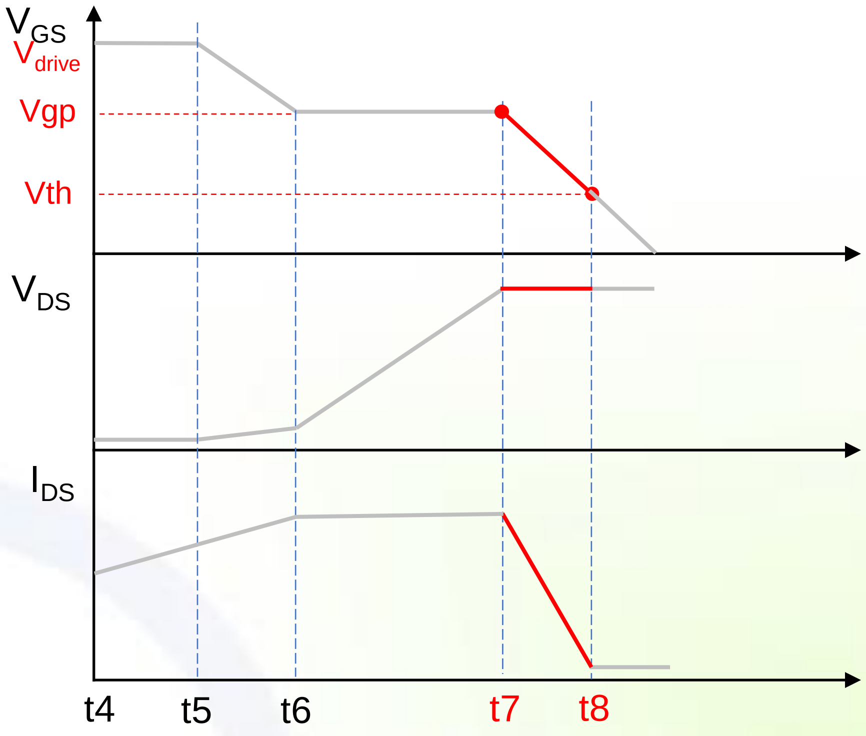


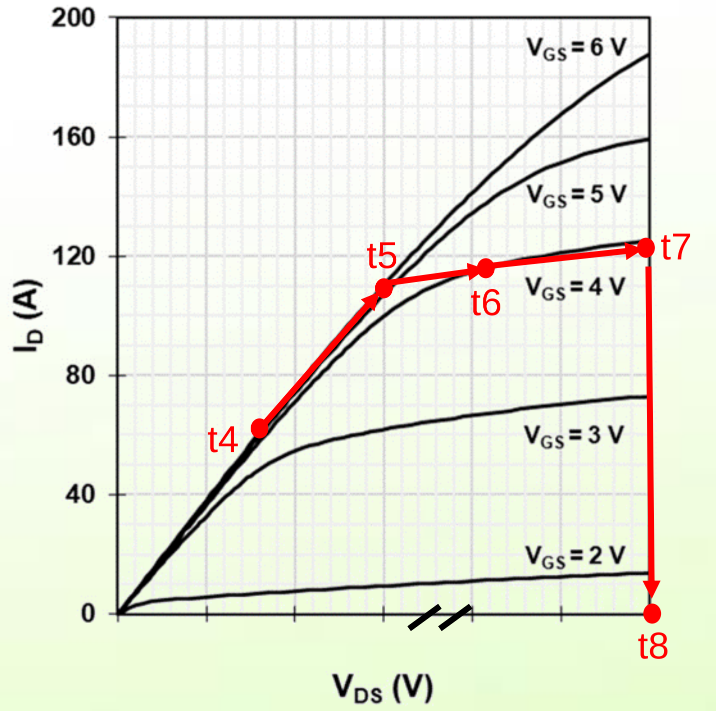
t6~t7, voltage commutation (Rec GaN V_{DS} rises to V_{bus}):

- Load current charges the switching node (charging C_{OSS} of Rec GaN, discharging C_{OSS} of Syn GaN)
- Parameter of Q_{OSS} is crucial, and determines charging/discharging speed (i.e. switching speed)
- Power loss on Rec GaN mainly comes from **I-V overlap loss**

HSW turn-off transient: current commutation





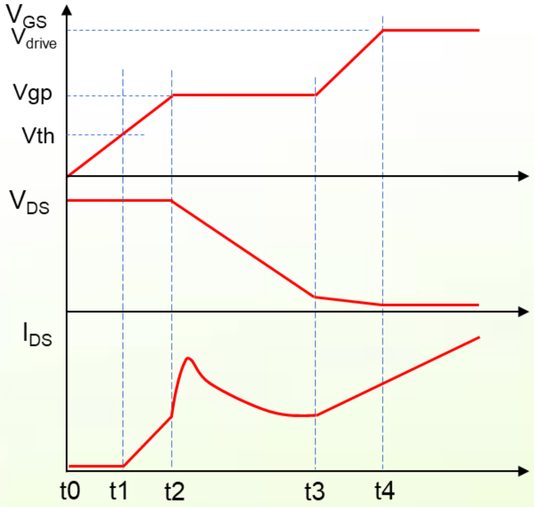


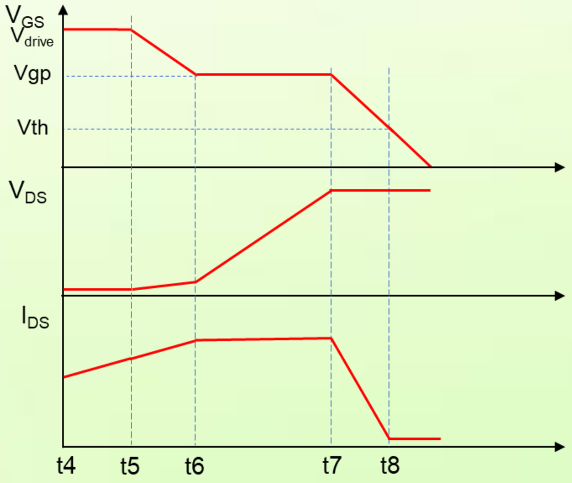
t7~t8, current commutation [load current commutates from Rec GaN to Syn GaN]:

- As V_{GS} of Rec GaN drops from Vgp, load current gradually commutates from Rec GaN to Syn GaN, as V_{GS} decreases;
- During current commutation, the gate driver discharges Ciss until Rec GaN has been turned off (V_{GS} = Vth)
- When Rec GaN V_{GS} = Vth (i.e. after t8), all the inductive-load current flows through the Syn GaN.
- Power loss mainly comes from **I-V overlap loss**

Summary

	V_{GS}	V_{DS}	I_{DS}	P_{loss} on Rec GaN	Loss from
Turn-on transient	Vgoff → Vth *Start to turn-on*	V_{bus}	0	~0 (V_{bus}*I_{dss})	Drain leakage
	Vth → Vgp *Current commutation*	V_{bus}	0 → I_L	$f_{sw} * \int I_{DS}V_{DS}dt$	I-V overlap
	Vgp *Voltage commutation*	V_{bus} → V_{ON}	I_L + $C_{(Vbus\text{-}VDS)}$*dv/dt	$f_{sw} * (\int I_{DS}V_{DS}dt + E_{oss})$	I-V overlap C_{OSS} of Syn/Rec GaN
	Vgp → V_{drive} *Gate fully turn-on*	V_{ON} ↓	I_L (dI_L = V_{bus}/L*dt)	$f_{sw} * \int I_{DS}V_{DS}dt$	Conduction loss
ON-state duration	V_{drive}	V_{ON} slightly rises (= I_L*R_{dson})	I_L (dI_L = V_{bus}/L*dt)	$\frac{Ip^2 + Iv^2 + IpIv}{3} * R_{dson} * duty$	Conduction loss
Turn-off transient	V_{drive} → Vgp *Start to turn-off*	V_{ON} ↑	I_L (dI_L = V_{bus}/L*dt)	$f_{sw} * \int I_{DS}V_{DS}dt$	Conduction loss
	Vgp *Voltage commutation*	V_{ON} → V_{bus}	I_L	$f_{sw} * \int I_{DS}V_{DS}dt$	I-V overlap
	Vgp → Vth *Current commutation*	V_{bus}	I_L → 0	$f_{sw} * \int I_{DS}V_{DS}dt$	I-V overlap
	Vth → Vgoff *Gate fully turn-off*	V_{bus}	0	~0 (V_{bus}*I_{dss})	Drain leakage





More information of GaN FET loss calculation in switch-mode power supply could be found in application note CGAN004.

Powering the Dreams by CloudSemi GaN

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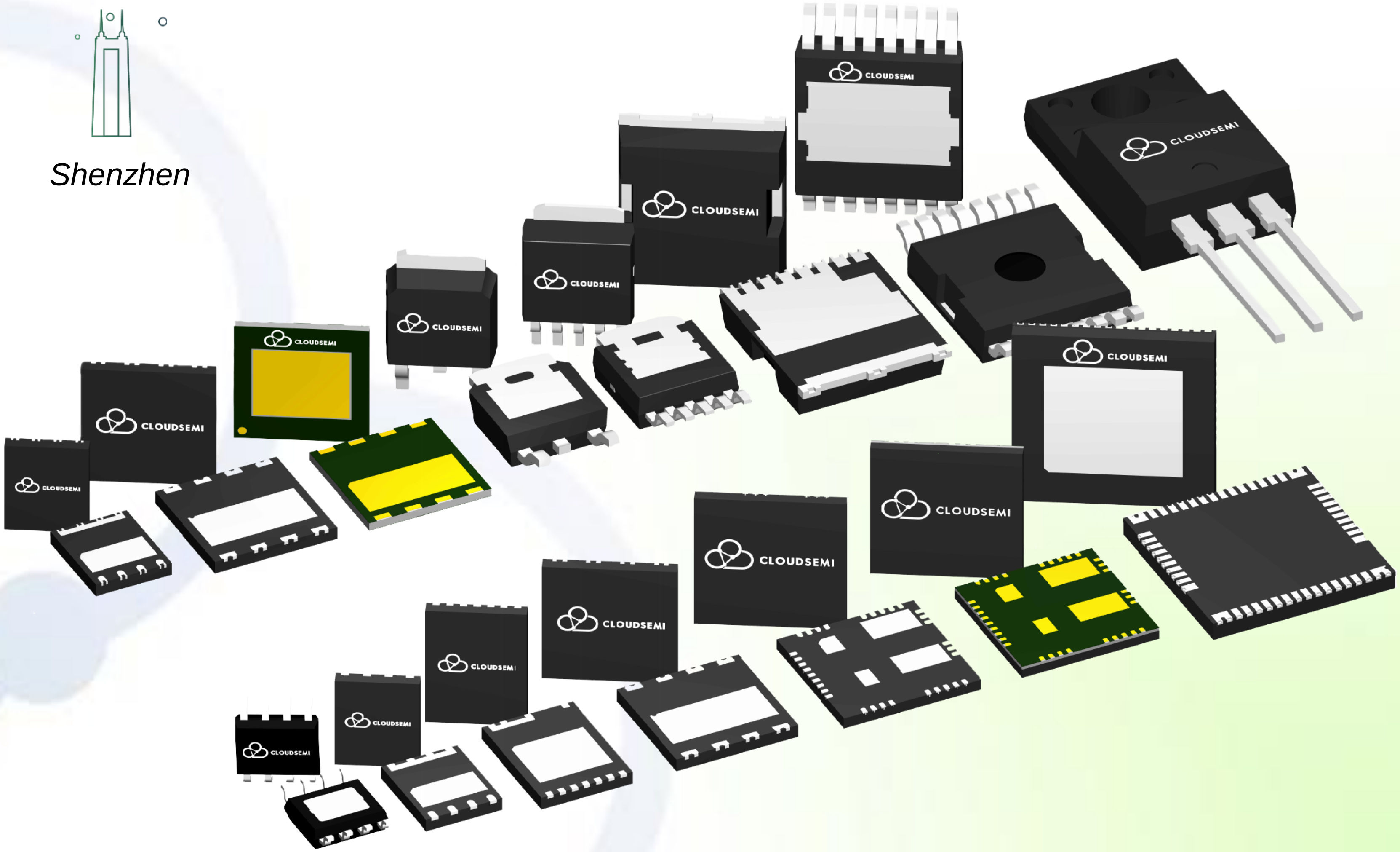

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Thank You!

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